Code No: **19ECT404** **R19**

II B. TECH II SEMESTER REGULAR EXAMINATIONS, AUG/SEPT 2021
DIGITAL SYSTEM DESIGN WITH VHDL
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

Note: Answer **ONE** question from each Unit (**5 × 12 = 60 Marks)**

UNIT - I

1.	a)	Implement the function of OR gate using emitter coupled logic and verify the operation with the help of its function table.	[6M]
	b)	Compare all the logic families in terms of different performance parameters.	[6M]

(OR)

2.	a)	What are the methods of CMOS-TTL interfacing in the case (i) CMOS driving TTL and (ii) TTL driving CMOS? Explain in detail.	[6M]
	b)	Explain the static and dynamic electrical behavior of CMOS circuit.	[6M]

UNIT – II

3.	a)	Develop the VHDL entity and architecture of the difference and borrow operation of the full-subtractor. Also draw its logic diagram.	[6M]
	b)	Explain the VHDL elements: data types, data objects, operators and identifiers with an example for each.	[6M]

(OR)

4.	a)	Develop the VHDL programming model for a JK-flip-flop.	[6M]
	b)	Explain the VHDL programming model of any combinational logic circuit.	[6M]

UNIT – III

5.	a)	Define the EXIT statement in VHDL with an example.	[6M]
	b)	Compare VHDL with other procedural languages.	[6M]

(OR)

6.	a)	Discuss about the concurrent statement WHEN in VHDL.	[6M]
	b)	Explain the following (i) single and multiple processes (ii) variable and signal assignment statements.	[6M]

UNIT –IV

7.	a)	Implement 8×1 multiplexer using 2×1 multiplexers.	[7M]
	b)	Write a VHDL architecture outline for ALU to illustrate the use of procedure defined within a process. Procedure computes addition and subtraction on two values using CASE statements producing a result and a Flag indicating whether the result is zero.	[5M]

(OR)

8.	a)	Explain the working and operation of priority encoder.	[6M]
	b)	Explain the operation of comparators using truth table and draw the logic diagram.	[6M]

UNIT –V

9.	a)	Write a VHDL code for a 4-bit universal shift register.	[6M]
	b)	Explain the operation of Johnson counter, verify using the truth table.	[6M]

(OR)

10.	a)	What is the difference between the latches and flip-flops? Implement a JK flip-flop using SR flip-flop.	[7M]
	b)	Write a VHDL code for sequence detector which detects 1011 overlapped sequence.	[5M]

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